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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,243	09/03/2003	Woo-Hyun Kim	041993-5232	2820

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EXAMINER	
VU, PHU	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/653,243	KIM, WOO-HYUN	
	Examiner	Art Unit	
	Phu Vu	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1-24 is/are allowed.

6)☒ Claim(s) 25-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/1/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 25 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiki US 5946060.

Regarding claims 25, Nishiki teaches a liquid crystal display panel, comprising: a plurality of gate lines (fig. 2A elements 1A and 1B) arranged along a first direction on a first substrate; a plurality of data lines (fig. 2B element 2) arranged along a second direction on the first substrate to cross the gate lines to define a plurality of unit pixels; an insulating layer (fig. 2B element 9) disposed over the gate and data lines; a common electrode (figs. 1A-1B element 5A) disposed on a second substrate opposite the first substrate; a plurality of pixel electrodes (4A) each pixel electrode provided in each of the unit pixels partitioned by the gate line and the data line to form a first electric field between the common and pixel electrode; a plurality of side electrodes (5B) overlapping the data lines along a length direction of the data lines, the side electrode in the pixel being extended to a neighboring pixel (see fig. 2A element 5B) causing a second electric field with the pixel electrode to distort the first electrode field, wherein the insulating layer(9) is provided between the side electrode (5B) and the data lines (2)

and a width of the side electrode is greater than a width of the data lines. The reference does not explicitly reference first and second electrode fields, however any charged objects (electrodes) will generate an electric field between them, therefore, an electric field exists between the pixel and common electrodes which is considered the "first field." The mere presence of a side electrode will produce a second electric field which will influence (distort) the first field.

Regarding claim 27, Nishiki teaches the side electrodes overlapping the data lines which divide the pixels therefore they must be provided between adjacent pixels.

Regarding claim 28, Nishiki shows the side electrodes (5B) overlapping the gate lines (1A) (see fig. 2A) with an insulation layer between (see fig 2B 9 and 7).

Regarding claim 29, a pixel that is "divided" does not necessarily indicate a physical division. Therefore, interpreting the pixel as divided into left and right sections and the center region being the connection region meets this limitation.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiki in view of Kim US 5338240.

Regarding claims 26, Nishiki teaches all the limitations of claims 26, except forming the pixel and side electrodes of the same material. Kim teaches ITO (a transparent conductive film) that can be patterned by conventional photolithography techniques (column 1 lines 48-55). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art use ITO to enable patterning by conventional photolithography techniques.

Claim 30-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiki in view of Applicant's Admitted Prior Art (AAPA) in view of Kim US 5338240.

Regarding claims 30-31 and 33-34, Nishiki teaches a second substrate bonded to the first substrate (fig. 1A and 1B element 6b), a liquid crystal material (15) formed between the first and second substrates; a black matrix (14) formed on a surface of the second substrate aligned to the gate lines and the data lines, a common electrode (5a) formed on another surface of the second substrate upon which the black matrix and the color filter (13) layer are formed. Nishiki fails to teach an electric field partition formed on the second substrate in the form of ribs formed on the surface of the common electrode or a slit formed and a plurality of partitions formed on the first substrate between adjacent ones of the plurality of pixel electrodes and wherein the liquid crystal layer has negative dielectric anisotropy. AAPA teaches an electric field partition formed on the second substrate in the form or ribs (see related art fig. 1 element 25), or a slit (see related art fig. 2 element 36) formed between adjacent portions of the common electrode with a liquid crystal layer having negative dielectric anisotropy ([0011]) that achieves improved contrast ratio and response time ([0013] and [0016-0020] and [0028]). Therefore, it would have been obvious to one of ordinary skill in the art to apply electric field partitions and a negative dielectric liquid crystal layer to improve contrast ration and response time. Nishiki and AAPA fail to teach the side electrodes, pixel electrode made of a transparent conductive material including ITO however Kim teaches ITO as an electrode material that can be patterned with conventional

photolithography techniques. Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to use ITO in order to allow for patterning by conventional photolithography techniques.

Regarding claim 32, Nishiki teaches a liquid crystal material formed between the first and second substrates (see fig. 1A and 1B).

Regarding claim 35, Nishiki teaches a plurality of electric field partitions a plurality of electric filed partitions formed on the first substrate between adjacent ones of the pixel electrodes (see figs 1A and 1B elements 4b and 5b).

Regarding claims 36 and 38-39, Nishiki teaches a method of fabricating a liquid crystal display panel comprising: forming a plurality of gate lines (fig. 2A elements 1A and 1B), a plurality of data lines (fig. 3A element 2), and a plurality of TFTs (fig. 3A element 3A) on a first substrate; forming a passivation layer (fig. 2B element 9) on a surface of the first substrate upon which the gate lines, the data lines, and the TFT transistors are formed; forming a transparent conductive material (4b) on a surface of the passivation layer; forming a plurality of side electrodes (5b) extending along a length direction of the data lines and overlapping the data lines by patterning the transparent conductive material, the side electrode in the pixel being extended to a neighboring pixel; forming a plurality of pixel electrodes (4b) separated from the side electrodes by patterning the transparent conductive material, forming a black matrix (figs 1A and 1B element 14), a color filter (fig. 1A-1B element 13), and a common electrode (fig. 1A – 1B element 5a) on a second substrate; bonding the first and second substrates together aligning the pixel electrode to the common electrode (see fig. 1A or 1B); and forming a

liquid crystal layer (fig. 1A or 1B element 15) between the bonded first and second substrates, wherein a width of the side electrode is greater than a width of the data lines (see element 5b and 2a). The reference does not explicitly reference first and second electrode fields, however any charged objects (electrodes) will generate an electric field between them, therefore, an electric field exists between the pixel and common electrodes which is considered the "first field." The mere presence of a side electrode will produce a second electric field which will influence (distort) the first field.

Nishiki omits forming an electric field partition on the common electrode in the form of a rib or slit. APA teaches an electric field partition formed on the second substrate in the form or ribs (see related art fig. 1 element 25), or a slit by etching (see related art fig. 2 element 36) formed between adjacent portions of the common electrode ([0011]) that achieves improved contrast ratio and response time ([0013] and [0016-0020] and [0028]). Therefore, it would have been obvious to one of ordinary skill in the art to apply electric field partitions of ribs or slits on the common electrode to improve contrast ratio and response time.

Regarding claim 37, Nishiki teaches etching the passivation layer to expose the drain electrode portions of the TFTs (see column lines "contact hole" contacting the drain electrode).

Allowable Subject Matter

Claims 1-24 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Regarding claims 1-24, the prior art of teaches all of the recited structure of

independent claims 1 and 24 except side portions of side electrodes coplanar with side portions of the pixel electrodes along the surface of the insulating layer.

Nishiki teaches a liquid crystal display panel, comprising: a plurality of gate lines arranged along a first direction on a first substrate; a plurality of data lines arranged along a second direction on the first substrate to cross the gate lines to define a plurality of unit pixels; an insulating layer disposed over the gate and data lines; a common electrode disposed on a second substrate opposite the first substrate; a plurality of pixel electrodes each pixel electrode provided in each of the unit pixels partitioned by the gate line and the data line; and a plurality of side electrodes overlapping the data lines along a length direction of the data lines, the side electrode in the pixel being extended to a neighboring pixel, wherein the insulating layer is provided between the side electrode and the data lines and a width of the side electrode is greater than a width of the data lines. Nishiki fails to teach these side electrodes having side portions coplanar with the pixel electrodes as they are found on an insulating layer above the pixel electrodes. Kim as previously cited teaches side electrodes that overlap the data lines however the width of these electrodes is explicitly less than that of the data lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu Vu whose telephone number is (571)-272-1562. The examiner can normally be reached on 8AM-5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phu Vu
Examiner
AU 2871

ANDREW SCHECHTER
PRIMARY EXAMINER